AMENDMENT TO THE CLAIMS

Claims 1-4 (canceled)

Claims 5-13 (withdrawn)

Claims 14-15 (canceled)

Claim 16 (withdrawn)

Claims 17-25 (canceled)

Claims 26-34 (withdrawn)

Claims 35-39 (canceled)

40. (currently amended) A method of forming a programmable resistance memory element, comprising:

providing a first dielectric layer, said first dielectric layer having a sidewall surface;

~~forming a sidewall surface in said dielectric layer;~~

forming a conductive layer on said sidewall surface;

forming a second dielectric layer over said conductive layer;

forming a mask over an exposed top surface of said conductive layer;

removing a portion of said conductive layer to form a protruding portion of said conductive layer under said mask; and

forming a programmable resistance material ~~adjacent to at least a portion of~~ electrically coupled to said protruding portion.

Claim 41 (canceled)

42. (previously amended) The method of claim 40, wherein said removing step comprises etching said conductive layer.

43. (original) The method of claim 42, wherein said etching step comprises anisotropically etching said conductive layer.

44. (original) The method of claim 42, wherein said etching step comprises isotropically etching said conductive layer.

45. (previously amended) The method of claim 40, wherein said mask has a lateral dimension less than 1000 Angstroms.

46. (previously amended) The method of claim 40, wherein said mask is a sidewall spacer and forming said mask step comprises forming said sidewall spacer.

Claims 47-56 (withdrawn)

57. (currently amended) The method of claim 40, wherein said ~~forming said sidewall surface step comprises forming an opening in said first dielectric layer, said opening having said sidewall surface~~ sidewall surface corresponds to a sidewall surface of an opening in said first dielectric layer.

58. (currently amended) The method of claim 57, wherein ~~forming said conductive layer on said sidewall surface step comprises forming said conductive layer on~~ said conductive layer is formed on said sidewall surface and ~~on substantially all of said~~ on a bottom surface of said opening.

59. (original) The method of claim 40, further comprising:

after said forming said conductive layer step and before said forming said second dielectric layer step, removing a portion of said conductive layer.

60. (original) The method of claim 59, wherein said removing said conductive layer step comprises anisotropically etching said conductive layer.

61. (original) The method of claim 40, wherein said programmable resistance material comprises a phase change material.

62. (original) The method of claim 40, wherein said programmable resistance material comprises a chalcogen element.

Claim 63-69 (canceled)

Claims 70-78 (withdrawn)

Claims 79-81 (canceled)

82. (currently amended) A method of making an electrode for a semiconductor device, comprising:

providing a first dielectric layer, said first dielectric layer having a sidewall surface;

~~forming a sidewall surface in said dielectric layer;~~

forming a conductive layer on said sidewall surface;

forming a second dielectric layer over said conductive layer;

forming a mask over an exposed top surface of said conductive layer; and

removing a portion of said conductive layer to form a protruding portion of said conductive layer under said mask.

Claim 83 (canceled)

84. (previously amended) The method of claim 82, wherein said removing step comprises etch said conductive layer.

85. (original) The method of claim 84, wherein said etching step comprises anisotropically etching said conductive layer.

86. (original) The method of claim 84, wherein said etching step comprises isotropically etching said conductive layer.

87. (previously amended) The method of claim 82, wherein said mask has a lateral dimension less than 1000 Angstroms.

88. (previously amended) The method of claim 82, wherein said mask is a sidewall spacer and forming said mask step comprises forming said sidewall spacer.

Claims 89-97 (withdrawn)

98. (previously amended) The method of claim 82, further comprising the steps of:

forming a third dielectric layer over said protruding portion; and

removing a portion of said third dielectric layer to expose a top surface of said protruding portion.

99. (currently amended) The method of claim 82, wherein said ~~forming said sidewall surface step comprises forming an opening in said first dielectric layer, said opening having said sidewall surface~~ sidewall surface corresponds to a sidewall surface of an opening in said first dielectric layer.

100. (currently amended) The method of claim 99, wherein ~~forming said conductive layer on said sidewall surface step comprises forming said conductive layer on~~ said conductive layer is formed on said sidewall surface and ~~on substantially all of said~~ on a bottom surface of said opening.

101. (original) The method of claim 82, further comprising:

after said forming said conductive layer step and before said forming said second dielectric layer step, removing a portion of said conductive layer.

102. (original) The method of claim 101, wherein said removing said conductive layer step comprises anisotropically etching said conductive layer.